Fraunhofer IIS

ADC7b6GS055nm

7 Bit 6 GS/s Folding ADC

Key Parameters

- Resolution: > 6 bit (76 levels)
- Conversion rate: 4 to 6 GS/s
- Power consumption: < 300 mW
- Signal-to-Noise: > 30 dB (up to 3 GHz)
- Spurious-free dynamic range: > 33 dB (up to 3 GHz)
- Differential input voltage: +/- 450 mV
- Supply voltage core: 1.2 V +/- 5 %
- Supply voltage peri: 1.8 V +/- 5 %
- Operating clock: 6 GHz (rms jitter < 1.3 ps)
- Temperature range: - 40 °C – 125 °C

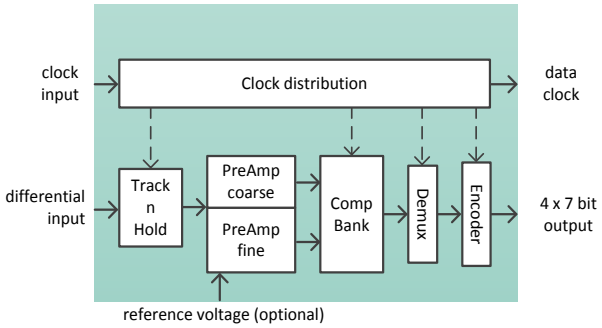

Fig. 1: IP-Level Block Diagram

General Description

The IP consists of a 7 bit monolithic folding ADC clocked externally for 6 GS/s.

The **differential input signal** of maximum +/- 450 mV is ac-coupled to the input. Lower cut-off frequency is well below 500 kHz.

The ADC is calibrated internally after reset to increase precision. The calibration can be disabled and can also be triggered manually.

The reference voltage is either derived from the 1.2 V supply or can alternatively be provided externally.

The IP needs an **external clock** with high accuracy and low jitter, because the clock jitter may influence the dynamic features of the converter. This clock is used as the sampling clock.

The digital output word of 7 bits is provided as a 4x parallel bus together with the clock.

The ADC is **silicon evaluated** in **Fujitsu 55 nm CS250L** technology.

Fraunhofer IIS provides a **detailed documentation** and **support** for the IP integration.
Modifications, extensions and technology ports of the IP are available on request.

Benefits

- Low design risk due to silicon evaluated design
- Robust operation across full temperature range from - 40 °C up to 125 °C
- Simple integration due to parallel digital interface with clock

Deliverables

- GDSII data
- Simulation model
- Documentation
- Integration support

FACT SHEET

CONTACT

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