An Integrated Overlay Architecture Based Multi-GNSS Front-end

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***Abstract*—This paper presents the overall architecture, first test structure implementations, and measurement results of an integrated GNSS front-end based on intentional path overlay. The front-end ASIC supports simultaneous multiband, multi-system GNSS reception of GPS L5 / Galileo E5 / GLONASS G3 and GPS L1 / Galileo E1 / GLONASS G1 signals with up to 52 MHz bandwidth while using only one common baseband path thanks to an intentional analog signal overlay. Test structures of the RF and baseband parts were realized in a 1.8 V, 150 nm RF-CMOS technology packaged in a QFN48 housings with full ESD protection. Both chips are described in detail regarding their design and their actual measurement results.**

***Index Terms*—Satellite navigation systems, Global Positioning System, Receivers, CMOS integrated circuits, GNSS front-end**

I. Introduction

Global navigation satellite system (GNSS) receivers greatly benefit from the modernization of existing GNSS constellations such as GPS and GLONASS as well as from the launch of new ones such as Galileo and COMPASS. First, the combining of these constellations can significantly improve the navigation solution availability in urban canyons and heavily shadowed areas. Second, increased satellite availability translates into higher measurement redundancy and improved reliability. Additionally, the excellent inherent noise and multipath mitigation capacity of the new and modernized wideband signals notably improves accuracy in both measurement and position domains.

Single-frequency users can receive GNSS signals and services but there are several advantages to multi-frequency processing: The frequency diversity offers superior protection against jamming and interference since, if one frequency band is corrupted, the receiver is still able to provide a navigation solution relying on another frequency band. Moreover a faster reception of the navigation messages is often possible since the same information is transmitted on several bands (e.g. the Galileo I/NAV message broadcast on both E1B and E5B) using page swapping [1]. Finally, multi-frequency can be used to form ionosphere-free pseudorange measurements that can remove the first-order ionospheric bias and therefore provide a higher positioning accuracy.

The challenges of multiband reception are a much higher required bandwidth, higher sampling rates, often several reception chains, a higher digital bandwidth (the raw sample rate from the front-end output to the baseband signal processing) and more self-generated interferences (e.g. when several frequency synthesizers for different local oscillator frequencies are needed). This all leads to a noticeable increase in receiver complexity, size, and power consumption, especially for integrated radio frequency (RF) front-ends.

Traditional GNSS front-ends but also current mass-market GNSS receivers typically feature a low intermediate frequency (low-IF) architecture with an RF-bandwidth of approx. 2 to 4 MHz and a low-resolution analog-to-digital converter (ADC) of 1 to 3 bit [2], [3]. This is sufficient for the legacy GPS L1 C/A or the narrowband Galileo E1 BOC(1,1) signals but not for most of the new GNSS signals, especially if their full potential in terms of accuracy and multipath resistance is to be reached. For these, considerably larger bandwidths are necessary (e.g. at least 16 MHz for the GPS/Galileo L1/E1 MBOC(6,1,1/11), 20 MHz for L5/E5A BPSK(10) signals, and up to 52 MHz for processing the complete Galileo E5 AltBOC(15,10) signal) which leads to higher sampling rate requirements.

The straightforward approach is to widen the bandwidth and to use higher sampling rates for each desired GNSS signal while keeping the original low-IF architecture. These solutions can already be found as integrated circuits and can easily be tuned to the required GNSS signal band [4], [5], [6]. However real multiband reception is only possible by adding a complete extra receiver for each additional frequency band to be received, either as a separate chip as proposed in [4] or by integrating more or less several standalone receivers on one die as proposed in [6] and [7]. This makes their implementation straight forward but is inefficient especially for an integrated circuit implementation.

For a wideband BOC signal such as the Galileo E5 AltBOC(15,10) a zero-IF architecture can be very advantageous since the inherent zero-IF problems, namely DC-offset and flicker noise, are not so relevant to the DC-free BOC signals. Moreover, quasi zero-IF architectures can be used to enable simultaneous reception of the L1/E1 GPS/Galileo signals and the GLONASS G1 frequency division multiple access (FDMA) signals by placing the local oscillator between both signal bands [8].

All the architectures mentioned so far are generic in a way that none exploit any properties of the GNSS signals code division multiple access (CDMA) structure: the useful signals are below the thermal noise floor, spread with long pseudo-random noise (PRN) sequences, and have different bandwidths. The complexity of a multiband RF front-end

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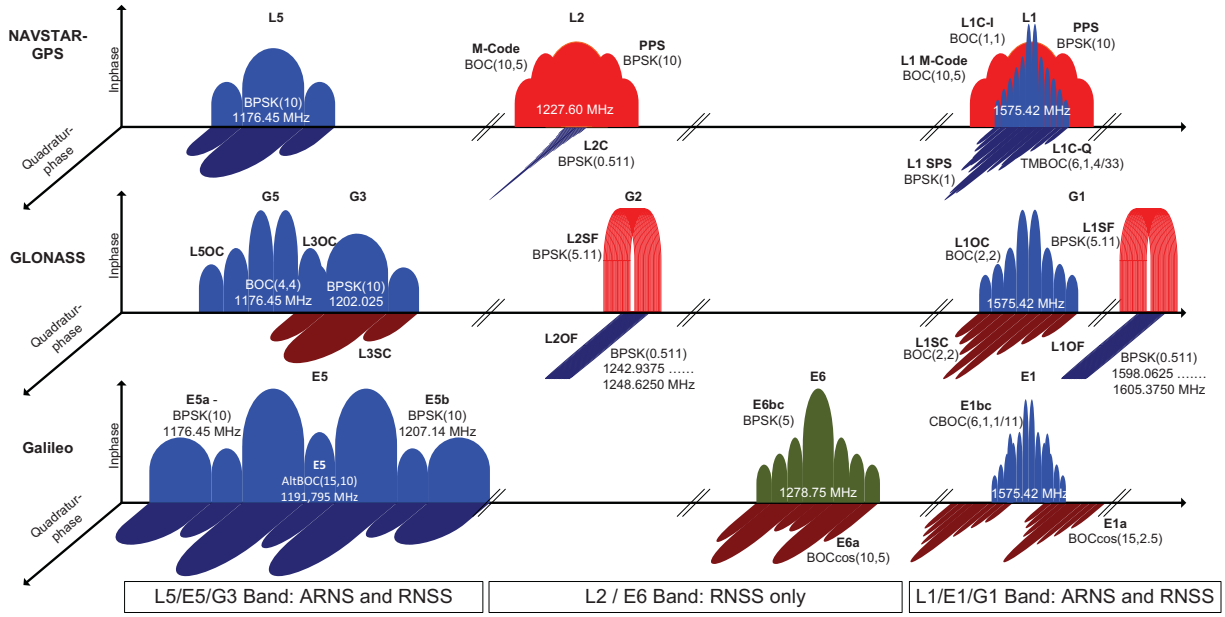

Fig. 1. GNSS signals of the future

can be considerably reduced by sharing front-end components or stages using intentional signal overlay while exploiting the aforementioned properties of the GNSS signals [9]. The proposed overlay front-end architecture exploits the properties of the direct sequence spread spectrum GNSS signals by intentionally overlaying two signal reception paths. Thanks to the overlay, only one common baseband path is needed. This allows significant savings in terms of cost, size, power consumption, and digital bandwidth. The possibility to receive wideband signals with up over 52 MHz bandwidth enables to fully benefit from the inherent noise and multipath resistance of the new Galileo AltBOC and GPS/Galileo MBOC signals. To the authors knowledge there are no publications of integrated GNSS front-end receiver chip measurements capable of processing the complete AltBOC signal.

The paper is organized as follows: First the selection of appropriate frequency bands for this receiver type is explained. Then the overlay architecture with its frequency plan and some implementation details is described. In the fourth section the used semiconductor technology of the ASIC is briefly introduced before the architecture and measurement results of both the RF and the baseband part are discussed in detail. Finally, conclusions are drawn and the performance of this overlay front-end is compared with that of current state-of-the-art integrated multi-GNSS front-end implementations.

II. GNSS Signals and Status

Currently, two fully operational GNSS are available: the American NAVSTAR-GPS and the Russian GLONASS system. Both systems are continuously evolving to improve the signals and services they will provide in the coming years. Aside, two other GNSS are being developed - the European Galileo and the Chinese COMPASS systems. Therefore, in a few years, at least four independent but interoperable GNSS will be available to support an increasing range of applications.

Figure 1 shows the L-band spectrum of the current and planned GNSS signals with the notation of their modulation names and carrier frequencies. The red and green signals are classified, the blue ones are open signals. All current and upcoming GNSS signals are within the protected Radio Navigation Satellite Services (RNSS) band but only the L1/E1/G1 and L5/E5/G5/G3 bands are within the even better protected spectrum allocated to Aeronautical Radio Navigation Services (ARNS). The other three GNSS bands (i.e. E6, G2, and L2) therefore suffer from radar, military transmissions and other potentially strong interferers.

The combination of both E5 (including the GPS L5, GLONASS L5OC and L3OC, Galileo E5a and E5b) and E1 (featuring the GPS L1 C/A and L1C, GLONASS L1OC, and Galileo E1-B/C) signals is deemed the most appropriate for the advanced open-service, multi-constellation, multi-frequency GNSS receiver that is intended to be realized with this integrated GNSS overlay front-end. For fast acquisition the relatively narrowband L1/E1 signals (GPS C/A and Galileo E1-B/C with BPSK(1) and BOC(1,1) modulation, respectively) are typically used. The estimated Doppler and code delay can then be used for high performance tracking with the wideband L1/E1 MBOC(6,1,1/11), L5/E5a BPSK(10), L5OC BOC(4,4) or E5b/L3OC BPSK(10) signals [10].

III. Overlay Front-end Architecture

The front-end architecture consists of a zero-IF down-conversion path for the L5/E5/G3 bands and a double heterodyne low-IF path for L1/E1/G1 bands as shown in Figure 2.

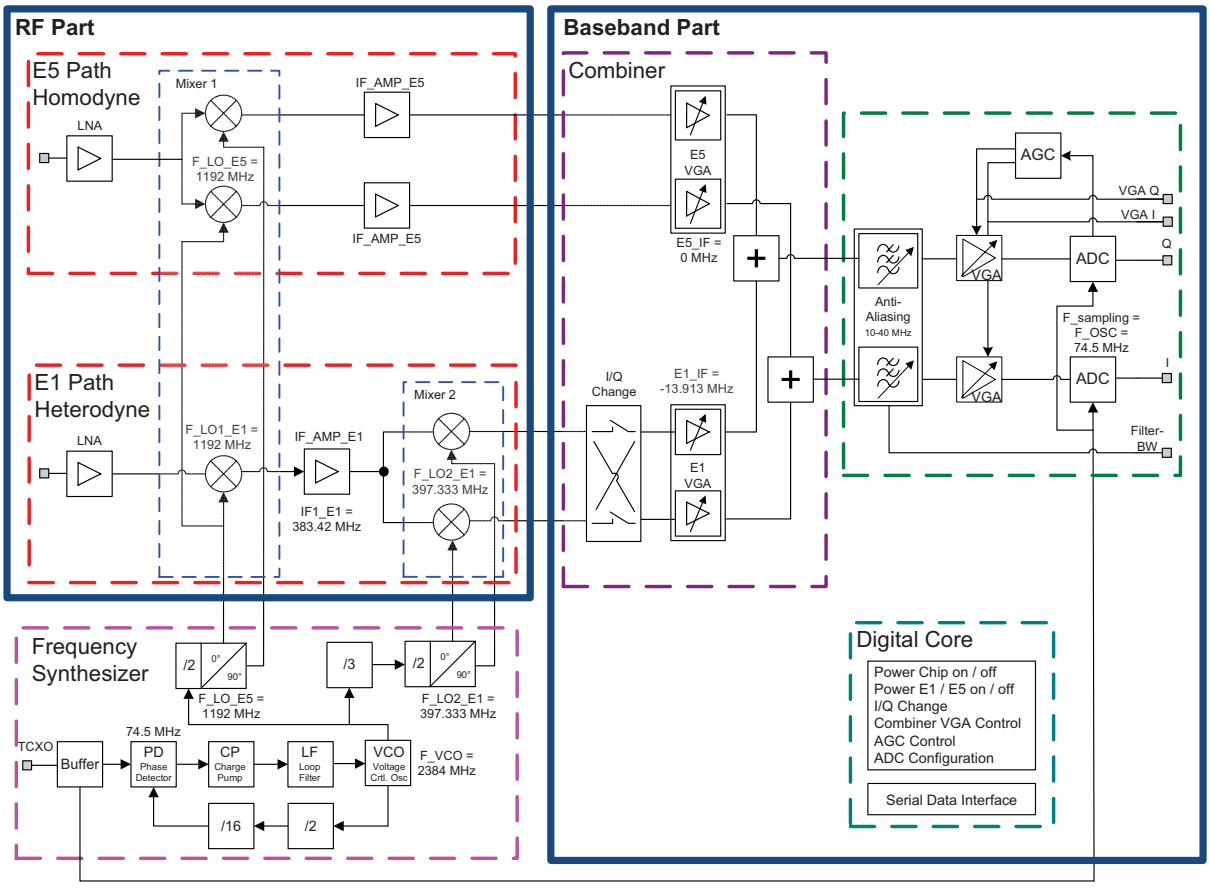

Fig. 2. Proposed overlay GNSS front-end architecture

The incoming L5/E5/G3 band is amplified and directly shifted to baseband by a quadrature down-conversion mixer with a local oscillator (LO) frequency of 1192 MHz and amplified again by an IF gain block.

A double heterodyne architecture is selected for the L1/E1/G1 reception path to circumvent the image problem of a pure low-IF architecture and to reuse the LO frequencies as it will be explained in the following paragraph. In the first mixing stage the RF signal is down-converted to an IF of approx. 400 MHz using a real mixer. The image frequency is more than 750 MHz away from the RF and can therefore be easily attenuated by an RF bandpass filter preceding the front-end input. An IF gain block both amplifies the IF signals and provides sufficient isolation to the next mixing stage. The second mixing stage consists of a complex mixer which shifts the IF signals to a low-IF frequency, as shown in Figure 3.

Thanks to a judicious frequency plan all LO frequencies can be directly derived with integer-N dividers from a single voltage controlled oscillator (VCO), as shown in the frequency synthesizer block diagram in Figure 2. This architecture reuses the E5-LO frequency for the first E1 mixing stage. The second E1 mixing stage uses exactly one third of the first E5-LO frequency. By using an off-chip reference oscillator of e.g. 74.5 MHz the frequency synthesizer can be realized with a straight forward integer-N PLL type implementation.

The combiner overlays both (complex) IF-signals from the E5/L5/G3 path and the E1/L1/G1 path in the analog domain. This is possible since all GNSS signals are direct sequence spread spectrum based signals with a high spreading gain and a negative signal-to-noise ratio (SNR) before the correlation. Preceding the overlay, the signals can be relatively amplified or attenuated using a variable gain amplifier (VGA) combiner controllable by the digital signal processing - in most cases the GNSS baseband receiver. Thanks to this combiner only one common baseband stage, consisting of an anti-aliasing lowpass filter, an automatic gain control loop (AGC), and analog-to-digital-converters (ADC) is needed.

The downside of the intentional signal overlay is that the noise from the overlayed signal bands is folded into the baseband range and directly affects the signals C/N_0. Using an appropriate power control before the overlay, the overlay noise can be controlled and at least partly mitigated as explained in [11]. Moreover, due to the overlay, jammers present in one frequency band also impact the other, previously undisturbed,

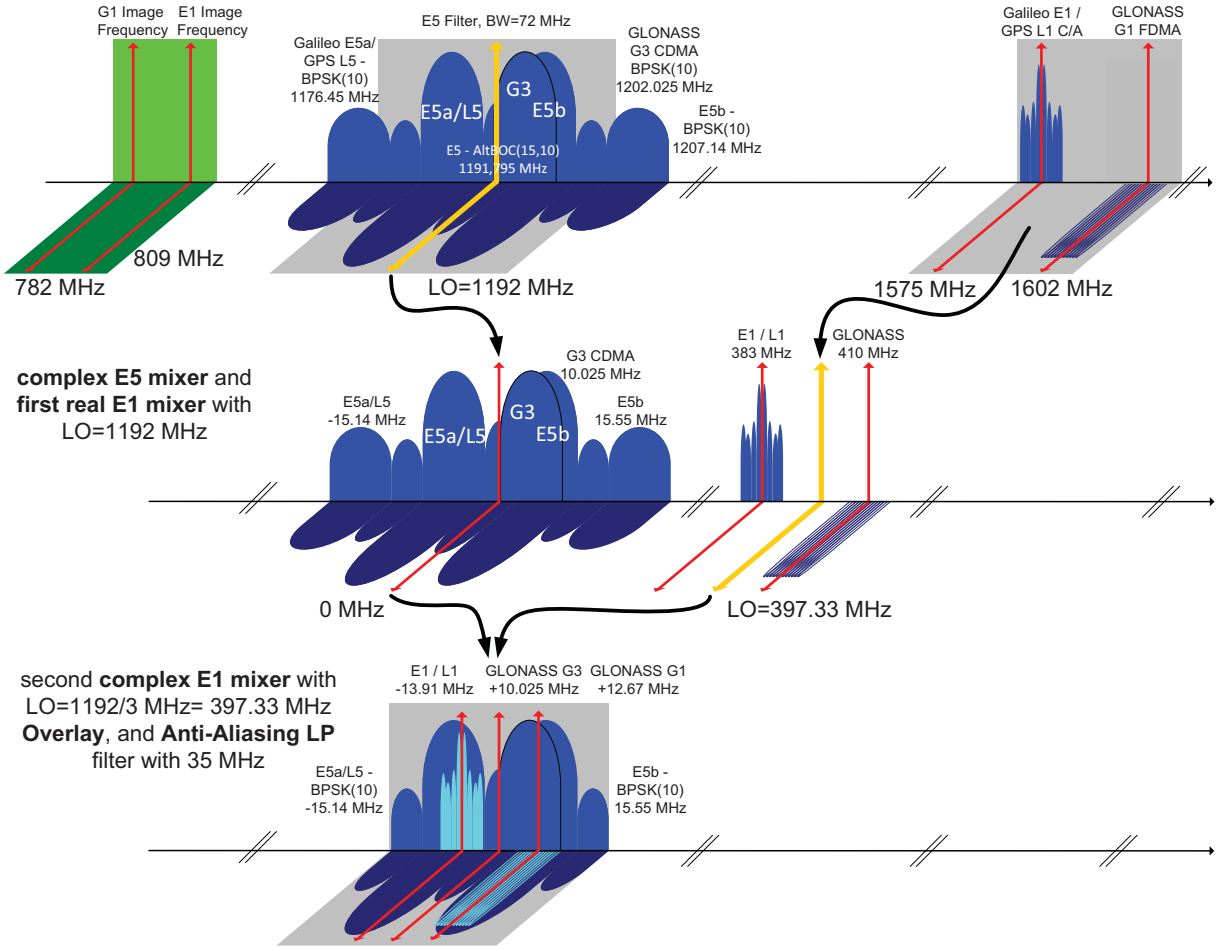

Fig. 3. Signal down-conversion scheme

frequency band. But the advantage of being able to receive all the open-service GNSS signals together with just one ADC is obvious and makes the overlay architecture interesting for advanced mass-market multiband, multi-system receivers.

IV. System and IC Design

For the integrated circuit implementation the new LF150 process from the German foundry *LFoundry* was used. LF150 features a 0.15 µm RF-CMOS process with up to 6 metal layers including a thick metal e.g. for high Q inductors and optimized RF library devices. The complete chip was implemented in this process using an 1.8 V operation supply.

To test and verify the different parts of this front-end architecture, its first implementation was split into three test structures described in the following sections: A low noise amplifier (LNA) and mixer "pipe-cleaner", an analog RF receiver part, and a mixed signal baseband part. These blocks are shown in Figure 2. The pipe-cleaner die was directly bonded on a printed circuit board (PCB) without any packaging while the other two test structure chips were packaged in a QFN48 housing including full ESD protection and measured on a dedicated PCB separately.

V. RF Part

It is assumed that an active antenna precedes the front-end chip. According to Friis' Formula, the active antenna LNA considerably lowers the noise figure (NF) requirements for the on-chip LNAs. The analog RF receiver test structure uses two fully differential LNAs for the upper and lower band amplification, followed by complex Gilbert mixing stages, intermediate amplifiers, and test-buffers to make off-chip measurements possible.

A. LNA, Mixer, and IF-Amplifier Architectures

For both the E1 and E5 band LNA a modified version of the fully differential topology described in [12] and [13] is used to significantly suppress on-chip interferences coming e.g. from the mixed signal baseband part on coupling over the substrate. The LNAs were not designed to achieve the lowest power consumption or NF but mainly for functionality. The LNAs consist of two stacked stages as shown in Figure 5. The

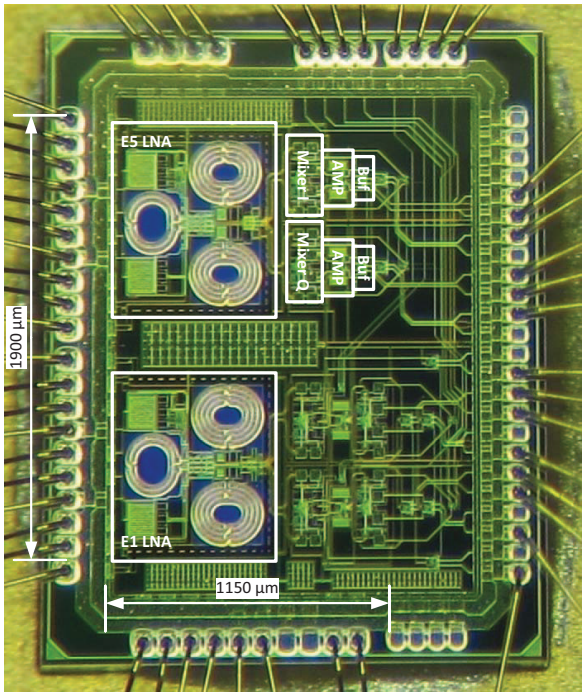

Fig. 4. Chip photo of the RF receiver test structure

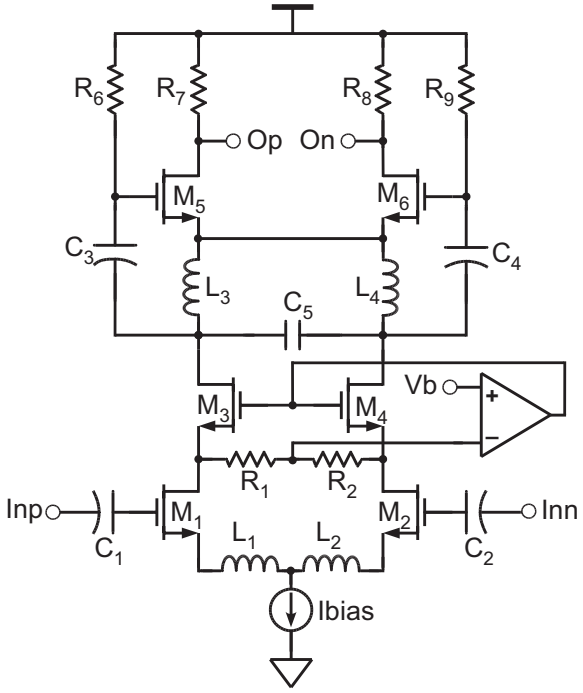

Fig. 5. LNA circuit diagram, modified version of [12], [13], some biasing details omitted

input stage is a cascode topology with transistors M_1 to M_4. A cascode topology is advantageous since it inherently provides a high reverse isolation [14] which is particularly important in the E5 zero-IF architecture, where the LO signal of the mixer matches the LNA's input frequency. For better input impedance matching an inductive source degeneration is used. Looking into the gates of the transistors M_1 and M_2 the inductors L_1 and L_2 contributes to the real part of the impedance. Instead of using two separate inductors a common tapped one is used, see the chip photo in Figure 4. With the series connection of the capacitor C_1 and C_2, and the real parts of the impedance seen through the gates of M_1 and M_2, respectively a highpass RC-filter is formed. The inductors L_3 and L_4 are used to tune the output of the first stage. The capacitor C_5 together with L_3 and L_4 sets the resonance frequency to the signals carrier frequencies. The differential amplifier between V_b and R_1 and R_2 adaptively controls the bias points and effectively mitigates process, temperature, and supply variations. A common-source output stage of the LNA is formed by the transistors M_5 and M_6.

Both the first and the second mixers are realized in a standard Gilbert-Cell topology. Gilbert-Cells are a fully differential, double balanced topology providing a very high LO to IF isolation [14]. Being fully differential fits perfectly to the differential LNA output. The high isolation is very beneficial for the intended E5 zero-IF architecture.

The IF-amplifiers are standard source coupled differential pairs with a resistive load designed for a gain-bandwidth product (GWB) of approx. 10 GHz. A coarse lowpass filtering at the output is realized with first order RC-filters.

B. RF Part Measurement Results

These analog RF components are most critical and at the same time crucial for the whole receiver functionality. To check the behavior of the design kit's RF-models a first "pipe-cleaner" run was done with test-structures of the LNAs and mixers already including full ESD protection. For the measurements the originated chip-die was directly bonded on a PCB without any packaging.

In order to measure the differential LNA input with a standard single-ended network analyzer, an RF-balun was used to convert between the single-ended and differential signal domains. Moreover the LNAs were matched using a lumped component LC-network before the balun. The measurement results of the input reflection coefficient S11 are shown in Figure 6 for both the lower band E5 and upper band E1 LNA with plots of the theoretical, normalized power spectral density (PSD) of the GNSS signals to be received. It can be seen that the 3 dB matched frequency bandwidth is greater than 200 MHz for both LNAs, enabling the reception of all the lower and upper GNSS L-band signals.

The impedances on the chip components are generally not designed for 50 Ω interfaces. The on-chip structures are so small in relation to the lower GHz frequencies in the L-band that any transmission line effects can be neglected. Therefore the on-chip LNAs outputs are not intended to drive a 50 Ω load, e.g. given by the standard measurement equipment. These LNAs only need to drive the much higher

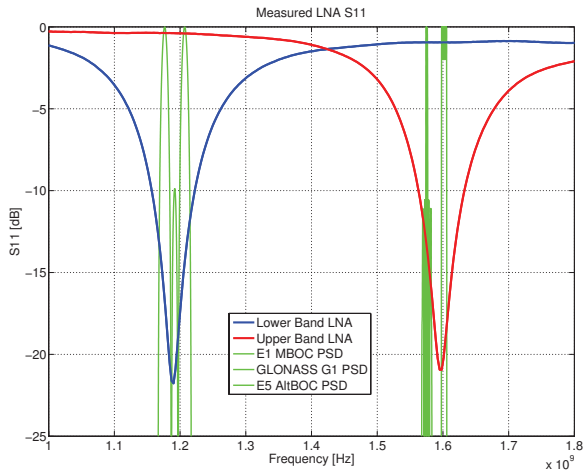

Fig. 6. Measured S11 of the lower band E5 and upper band E1 LNA with plots of the theoretical, normalized PSD of the GNSS signals to be received

impedance of the following active mixer stage. To enable off-chip measurements, a NMOS buffer with a transconductance of 20 mS was designed at the output of the mixer leading to 0 dB gain when a load impedance of 50 Ω is applied. Designing such a buffer for the mixer output is facilitated by the fact that the mixer output frequencies are within the IF range and no longer are at RF.

Therefore, the gain of the LNA can only be measured indirectly. First the gain of the active mixer was determined to be 9.5 dB for both the E1 and E5 mixers using the NMOS-buffer as previously explained. The active mixer LO input was an external rectangle signal with a differential peak-to-peak amplitude of 700 mV. Then the complete chain including the LNA and mixer was measured. The implementation losses of the balun and cables were deembedded. With the previously determined mixer gain, the LNA gain alone could be calculated. The results of the pipe-cleaner measurements of the LNA and mixer are shown in Table I and fit to the simulated values. The current consumption is around 3 mA for the E5 LNA, and around 2 mA for the E1 LNA, which is also consistent with the simulations.

The 1 dB input compression point of the combined LNA with mixer measurement was determined to be −30 dBm for both E1 and E5. In comparison to the linearity of off-the-shelf LNAs this may seem very low, but keeping in mind that in an undisturbed environment only thermal noise within the bandwidth of interest is received (approx. −100 dBm) and that the front-end incorporates a 3 bit ADC which provides approx. 18 dB of dynamic, even a −30 dBm input compression point is sufficient.

Having validated the pipe-cleaner designs, the complete RF receiver including the intermediate frequency amplifier was manufactured and packaged in the intended QFN48 housing. A photo of the chip is shown in Figure 4. Still the aforementioned buffers are included in parallel to each component's output for this test structure to allow separate component measurements.

TABLE I
MEASUREMENT AND SIMULATION RESULTS OF THE RF RECEIVER COMPONENTS

	E5 LNA[1]	E1 LNA[1]	Mixer[1]	IF_AMP[2]
Gain sim. [dB]	20.0	15.0	10.0	15.0
Gain meas. [dB]	19.0	12.0	9.5	16.0
NF sim. [dB]	<4	<4	13.75	13.04
Pin1dB meas. [dBm]	-30	-30	-5	
Current sim. [mA]	2.5	1.5	3.2	5.3
Current meas. [mA]	3.1	2.0	3.1	

[1] Measurement results from pipe-cleaner test structure
[2] Measurement results from RF part test structure

TABLE II
SIMULATION RESULTS OF THE BASEBAND COMPONENTS

	Combiner	LP Filter	AGC/VGA	ADC
Gain [dB]	−10 to 15	0	−12 to 40	-
Current (typ.) [mA]	12.4	27.1	19.7	7.0

The measurements of the RF receiver test structure confirmed its functionality but its gain was approx. 10 dB lower than expected based on the pipe-cleaner measurements. The IF-amplifier was approved as predicted by the simulations. After some separate component measurements it was concluded that the low gain was caused by both the E1 and E5 LNAs. Unfortunately, the reason for this cannot be exactly determined since the German *LFoundry* subsidiary went out of business shortly after delivering the chips. However, it can be assumed that this probably was a coincidence, e.g. some chances in the process parameters which were not sufficiently represented in the last version of the design kit. This theory seems to be confirmed by the fact that a variable controlled oscillator (VCO) which had previously been successfully measured was no longer oscillating at the right frequency in the frequency synthesizer test structure.

VI. BASEBAND PART

The mixed signal baseband part consists of a combiner with adjustable combination ratios, adjustable anti-aliasing lowpass filters, an AGC with over 50 dB dynamic range and a 3 bit, 74.5 MHz dual-ADC with integrated pulse blanking capability. The baseband blocks are shown in Figure 2.

By using an integrated serial peripheral interface (SPI) controller, the SNR degradation resulting from the combination of both signal paths can be minimized by setting the relative combiner gain to an appropriate value. This method was described in [11]. Moreover the SPI controller can be used to enable different power down features.

Figure 7 shows a chip photo of the baseband part. The core layout was already structured for an optimized complete integrated front-end chip. The baseband part size is smaller than 0.91 mm^2. For this test structure only, the spaces were filled with on-chip blocking capacitors. All the components are powered by 1.8 V. The power consumption is summarized in Table II.

A. Baseband Component Description

1) Digital Core: A digital core featuring an SPI was implemented within the baseband part. It can control, configure,

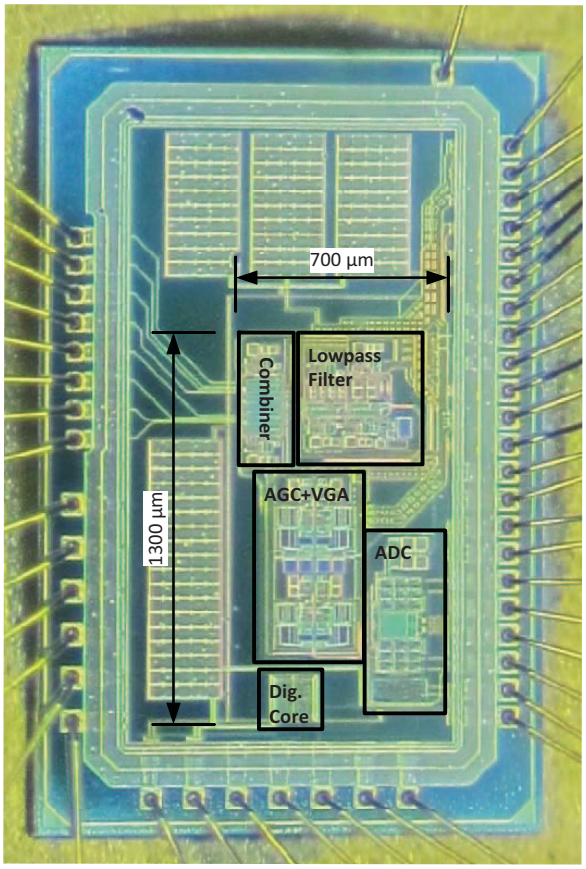

Fig. 7. Chip photo of the baseband part

TABLE III
DIGITAL CORE FUNCTIONALITY

Logical Block	Component	Method
LNA	E1	Power Down
	E5	Power Down
Mixer	E5 I and/or Q	Power Down
	First E1 I and/or Q	Power Down
	Second E1 I and/or Q	Power Down
IF-amplifier	E5 I and/or Q	Power Down
	E1 I and/or Q	Power Down
Combiner	I/Q Change	Mirror E1 Spectrum
	VGA E1 6 bit	−10 to 15 dB
	VGA E5 6 bit	−10 to 15 dB
	Adder I and/or Q	Power Down
AGC	Low-pass Filter	Power Down
	ADC VGA I and/or Q	Power Down
	Internal AGC Loop	Power Down
	Control Method	CW or GNSS-noise
	Pulse Blanking	on / off
	Overload Control	on / off
ADC	I and/or Q Path	Power Down
	ADC Buffer	Power Down
	Resolution	3 or 2 bit
	Output Format	
	Output Driver Strength	

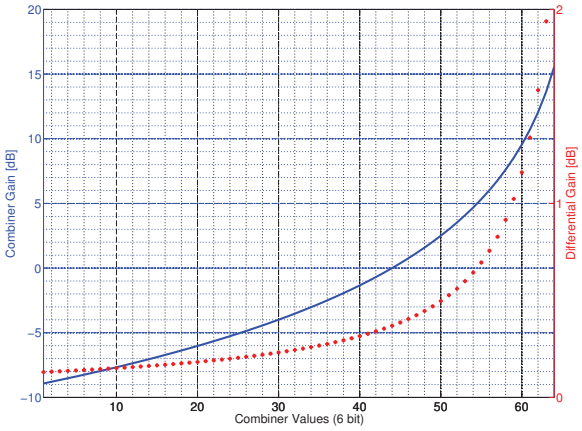

Fig. 8. Simulation of the combiner block digital programmable gain for both E1 and E5 paths

and turn off various blocks and components of the chip. Its functionality is summarized in Table III. The digital core not only allows an effective debugging and testing of the chip, it also gives to the GNSS receiver the possibility to modify or control the front-end hardware according to its environment e.g. switching off one path if a severe interferer is detected or controlling the combiner gain values to minimize the overlay loss as described in [11].

2) Combiner: As shown in the combiner block diagram in Figure 2, before the E1 and E5 signal paths are overlayed they can be amplified or attenuated by the combiner VGA cell. This block can be controlled in 64-steps (6 bit) via the SPI-bus of the digital core. Each signal path has a tunable 25 dB dynamic range from −10 to 15 dB, see Figure 8. In order to improve the area implementation of the cell, the steps show a non-linear characteristic depicted as differential gain in Figure 8. Since the combiner VGAs should be regulated by an adaptive control algorithm running on the baseband GNSS receiver, this non-linearity is irrelevant.

According to the frequency down-conversion scheme depicted in Figure 3 the E1 signal overlays the E5a/L5 main lobe. If the RF-filter exclusively selects the E1 frequency band, only the left main-lobe of E5 (in essence the Galileo E5a and GPS L5 signals) is affected by the overlay while the right main-lobe comprising Galileo E5b remains untouched. This can also be inverted by changing either the polarity of one E1 signal I/Q component (swapping + and - signals in the in-phase and quadrature branch) or its phase (swapping the in-phase and quadrature branch) before the combiner stage. Doing so leads to a mirroring of the E1 signal around the zero frequency axis. Depending on the intended application, this method can be beneficial since the overlay loss can be completely switched off on either E5a or E5b assuming an adequate E1 signal RF bandpass filter.

3) Anti-Aliasing Lowpass Filter: A 4th order active lowpass filter was realized in a Chebyshev topology using two op-amps and RC-networks. The default 3 dB cutoff frequency is around 33 MHz. Since the bandwidth setting integrated RC values vary by ±20 % due to CMOS process variations a self-calibration was realized with an external reference

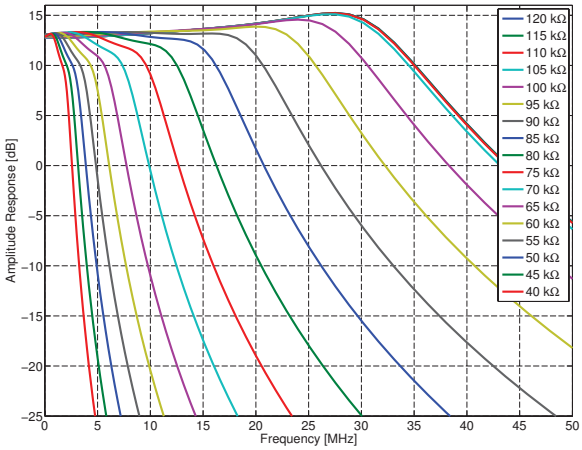

Fig. 9. Simulation results of the low-pass filter bandwidth together with the combiner in dependency of an external reference resistor

resistor. This external resistor can also be used to adjust the filter bandwidth between 3 to 35 MHz. Figure 9 shows the simulation result of the filter bandwidth in dependency of the external reference resistor value swept from 40 to 120 kΩ.

4) Automatic Gain Control: The automatic gain control ensures that the ADC's input signals are within the optimal range. The AGC senses the distribution of the ADC bits and sets the ADC VGA gain appropriately. The control algorithms can be configured to achieve better performance in presence of CW signals or for a minimum C/N_0 loss when GNSS-noise like signals are applied. The dynamic range of the VGAs is −12 to 40 dB according to the simulations.

5) Pulse Blanking: The baseband chip is equipped with an energy detector setting a blanking flag output signal if ADC clipping is occurring. Moreover, the ADCs can be configured to blank the signal if the blanking flag is active. This feature enables pulse blanking mitigation at a very early stage making it very effective. Finally, the AGC can be protected from being stimulated from pulses using the overload control switch.

6) ADC: The analog-to-digital-converters (ADC) digitize the output differential signals of the variable gain amplifiers. Typical GNSS receivers use low bit quantization. The implemented converters employ 3 bit which is a good trade-off between complexity and low implementation loss. Due to the low number of bits requirement, the classical flash topology was selected. The cell includes a buffer, a resistor ladder, comparators and a digital core cell for decoding. The components are optimized in terms of current consumption and speed. The comparators include an amplification stage and a decision stage. The amplification stage reduces the coupling to the input signal of the noise generated at the decision stage. The decision stage consumes current only at the rising edge of the clock signal. The current consumption of the different stages is minimized in order to preserve the ADCs linearity. The resistor ladders of the ADCs are placed together in the layout in order to reduce the mismatch.

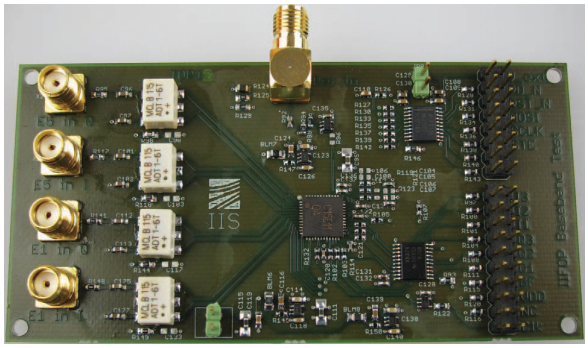

Fig. 10. Photo of the baseband part test PCB

B. Baseband Measurement Results

The baseband functionality was measured and verified with the test board shown in Figure 10. The PCB provides two complex input signals (E5 I/Q, E1 I/Q) which are converted from single-ended to differential with an external balun including a bias point. Moreover some output buffers for the clock input, the digital ADC outputs, and SPI interface are employed as an interface for the measurement equipment.

It has to be noted that due to the baseband part test structure implementation, it is not possible to test single blocks separately. Therefore, all reported test results were measured at the dual-ADC outputs using input signals at the combiner. The measurement results include all effects from all the baseband part components (from combiner to ADCs).

1) Combiner: To test the combiner with its E1 and E5 VGAs, two complex GNSS baseband signals - one 16 MHz bandlimited E1 MBOC and one E5 AltBOC signal - were generated and fed to the baseband part inputs with a high SNR to be able to identify their main-lobes in the plots. The E1 signal was shifted to an IF of −13.91 MHz to be compliant with the frequency down-conversion scheme proposed in Figure 3. Using the combiner VGAs, the E1 signal amplification was varied from 13.5 to −5.3 dB while the E5 combiner VGA was hold constantly on 2 dB. Figure 11 shows the overlayed signals with different E1 combiner VGA settings. Since the AGC automatically amplifies the overlay output signal to fit to the optimum ADC range, the PSDs shown in Figure 11 were scaled in a way that the E5b main lobe is approximately always at the same level. This enables a better comparison of the combiner VGA effect. It can be concluded, that the overlay works appropriately and that sufficient overlay control of the path is provided by the implemented combiner VGAs.

2) E1 I/Q Change: The blue colored plot in Figure 12 shows the recorded PSD when both paths are simultaneously activated with intentional overlay of the E1 MBOC and E5a BPSK signals according to the frequency down-conversion scheme proposed in Figure 3. As the blue colored plot shows, the left main-lobe of E5a is completely affected by the overlay while the right side remains untouched. Activating the E1 I/Q change feature, only the E1 path is mirrored around the zero frequency axis. The PSD with activated E1 I/Q change is

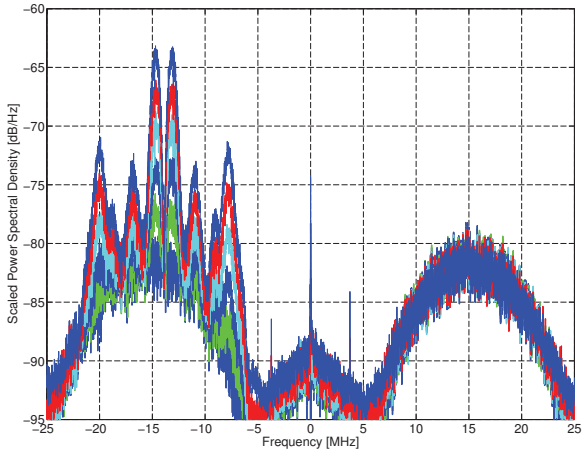

Fig. 11. Measured overlay PSD of E1 and E5 signals in dependency of the E1 combiner VGA settings

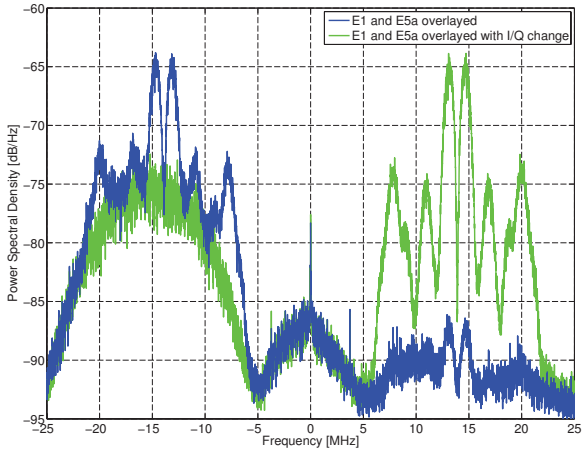

Fig. 12. Measurement of E1 I/Q change activation

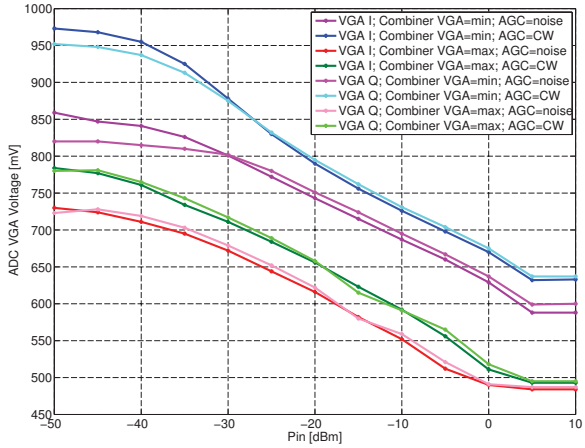

Fig. 13. Measured ADC VGAs values of the I and Q paths in dependency of the input power

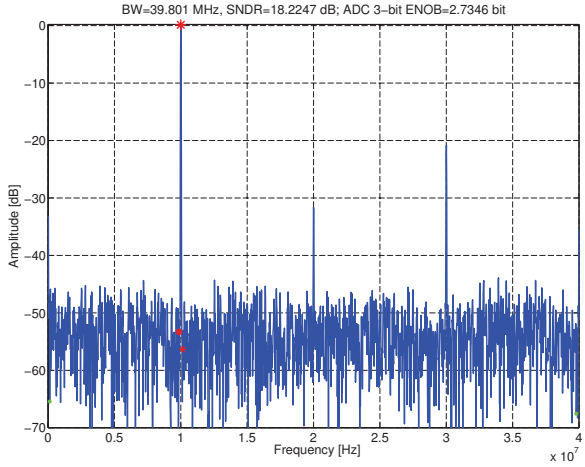

Fig. 14. Measured dual-ADC output spectrum with 10 MHz input tone and a sampling frequency of 80 MHz

depicted in the same Figure in green color and shows that the E5a main-lobe is now no longer affected by the overlay.

3) AGC and ADC VGAs: The AGC loop continuously modifies the ADC VGAs control voltage to guarantee an optimal ADC input power. The implemented circuitry enables to control the VGAs (I and Q) independently or together, as shown in Figure 2. The voltages at the I and Q VGA control pins were measured while the input power was swept. The AGC loop controls the VGAs in a way that the ADC input power is kept constant. Therefore, the VGAs dynamic range can be measured observing the range of the control voltages to be approx. 50 dB between the signal input powers of 5 to −45 dBm as shown in Figure 13. However, it should be noted that for normal operation the I and Q VGA control pins are connected together. Nevertheless Figure 13 also demonstrates the excellent matching of the I and Q baseband paths.

Moreover, the combiner VGAs were set to their minimum value (approx. −10 dB) and afterwards to their maximum value (approx. 15 dB). The combiner VGAs dynamic range can also be confirmed by measuring the offset between the results with minimum and maximum combiner VGAs settings.

And finally, the AGC control method was changed from CW-mode to the GNSS-noise mode. In CW-mode more clipping of the ADCs occurs. Therefore the VGAs gain in CW AGC mode is always approx. 5 dB higher than in the GNSS-noise mode.

4) ADC: Figure 14 shows the measurement results of the signal-to-noise-and-distortion-ratio (SNDR) of the whole baseband part at nominal conditions. A 10 MHz input signal was applied to the test-chip and sampled with 80 MHz. Using Equation 1 for a sinusoidal input signal, the effective number of bits (ENOB) was calculated to be 2.74 bit which is in accordance with the simulation results.

$$\text{ENOB} = (\text{SNDR} - 1.76\,\text{dB})/6.02\,\text{dB} \qquad (1)$$

Although the receiver architecture shown in Figure 2 has a nominal dual-ADC sampling rate of 74.5 MHz, different tests

TABLE IV
COMPARISON WITH PREVIOUSLY PUBLISHED INTEGRATED MULTIBAND GNSS FRONT-ENDS

	[4]	[15]	[5]	[7]	[6]	[8]	this work
Process	130 nm CMOS	180 nm CMOS	65 nm CMOS	130 nm CMOS	180 nm CMOS	65 nm CMOS	150 nm CMOS
1st GNSS band	L1/E1	L1/E1	L1/E1	L1/E1	L1/E1/B1,	L1/E1/B1,	L1/E1/G1
2nd GNSS band	L5/E5a[a]	L5/E5a [b]	G1	L5/E5a[c]	L5/E5a, B2/E5b	B2/E5b	L5/E5a, E5b/G3
3rd GNSS band	-	-	-	-	L2 [c,d]	L2 [c,d]	E5
Bandwidth	14/20 MHz	9 MHz	2/4/8 MHz	4.53/24 MHz	2/4/20 MHz	2 to 8 MHz	52 MHz
ADC resolution	2 bit	I/Q , n.a.	2x 3 bit	2 bit	4 bit	I/Q 2 to 4 bit	I/Q 3 bit
ADC sampl. rate	66.188 MHz	24 MHz	32.736 MHz	49.104 MHz	62 MHz	n.a.	74.5 MHz
Size	2.89 mm^2 [a]	16.0 mm^2	4.65 mm^2	11.4 mm^2	7.2 mm^2	10.5 mm^2	6.76 mm^2 [e]

[a] One chip needed for each GNSS band to be received
[b] Switching receiver architecture; only one band can be received at the same time
[c] Integration of two almost independent reception chains
[d] Only two GNSS bands can be received simultaneously
[e] Die size of complete receiver including frequency synthesizer

showed a reliable maximum ADCs sampling rate of over 150 MHz.

VII. CONCLUSION

The presented RF front-end parts enable the simultaneous reception of GPS L5 / Galileo E5 / GLONASS G3 and GPS L1 / Galileo E1 / GLONASS G1 signals with broad bandwidth. By using the proposed frequency plan and sharing the baseband parts with an overlay concept, the underlying architecture enables an efficient implementation in terms of digital data rate, chip size, and power consumption.

In comparison to other recently published integrated multi-GNSS front-end implementations (see Table IV) the reception bandwidth has been significantly increased. The presented implementation supports the first time the reception of the complete 52 MHz bandwidth Galileo E5 AltBOC(15,10) signal in an integrated front-end enabling to fully benefit from the inherent noise and multipath resistance of this sophisticated modulation scheme.

For future work, the presented RF and baseband parts will be revised and combined with the frequency synthesizer to form a fully integrated multi-GNSS front-end ready to coherently and simultaneously receive most open GNSS signals. The currently foreseen layout of the complete receiver chip including the frequency synthesizer has a die size of 6.76 mm^2. The already small implementation size shows the potential of this overlay architecture as compared to other recently published integrated multi-GNSS front-end architectures.

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