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ADC11b100kS22nm

11 Bit 100 kS/s Ultra-Low Power SAR ADC

Key Parameters

- Resolution: 11 bit
- Conversion rate: 100 kSps
- Power consumption: 2.5 µW @ 0.8V
- ENOB: 8.8 bit
- Operation clock: 2.0 MHz
- Input voltage range: 0.4 V ± 0.35 V
- Operating temperature -40 – 125°C
- Technology: cmos22fdsoi

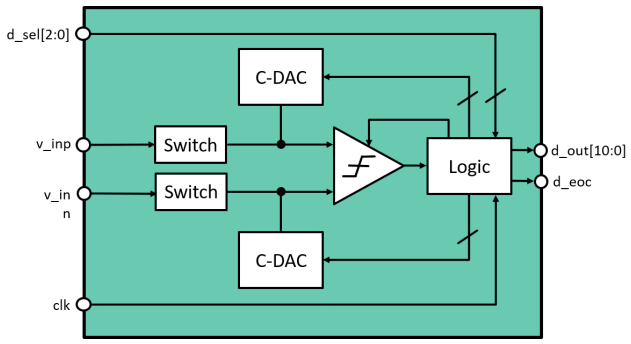

Fig. 1: IP-Level Block Diagram

General Description

The ADC IP is a general-purpose successive approximation converter for low-power medium-resolution applications. Sample rate, resolution and power consumption are configurable.

It is built using typical differential capacitor-DAC architecture, clocked comparator and bootstrapped switches. No additional reference voltage is required, achieving lmost rail-to-rail input. The target applications are environmental and biomedical signal processing.

The ADC is **silicon proven** using the GlobalFoundries 22FDSOI process. Measurement results and samples are available.

Fraunhofer IIS provides a **detailed documentation** and **support** for the IP integration. **Modifications, extensions and technology ports** of the IP are available on request.

Benefits

- Accelerated design service
- Design safety (first-time-right)
- Customer-specific flexible IPs
- Automated DfR and verification
- Seamless technology migration

Deliverables

- GDSII data
- Simulation model
- Documentation
- Integration and customizing support

FACT SHEET

CONTACT

Fraunhofer IIS

mixed-signal-ic-design@iis.fraunhofer.de

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