

A Bavarian Initiative towards a Robust Galileo PRS Receiver

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BIOGRAPHY

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Nikola Basta received his Dipl.-Ing. degree in 2008 at Faculty of Electrical Engineering at the University of Belgrade, Serbia. Since June 2008 he has been working in German Aerospace Centre (DLR) in the antenna group of the navigation department where he has been involved in design and characterization of antenna arrays for GNSS applications.

Michael Meurer received the diploma in electrical engineering and the Ph.D. degree from the University of Kaiserslautern, Germany. After graduation, he joined the Research Group for Radio Communications at the Technical University of Kaiserslautern, Germany, as a senior key researcher, where he was involved in various international and national projects in the field of communications and navigation. Since 2005 he has been an Associate Professor (PD) at the same university. Additionally, since 2006 Dr. Meurer is with the German Aerospace Centre (DLR), Institute for Communications and Navigation, where he is the director of the Department of Navigation and of the Centre of Excellence for Satellite Navigation.

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Melanie Kaindl graduated in 1998 in electrical engineering at the Aachen University of Technology. In 2005 she received her Ph.D. in communications engineering from the Munich University of Technology.

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ABSTRACT

This paper presents the architecture, core technologies, system development, and setup of the BaSE Galileo PRS receiver. The receiver is capable of processing Galileo E1/E6 PRS signals with broad bandwidth. In particular, its hard- and software receiver components are presented and a robust tracking method of the BOCc-modulated PRS signals is discussed. Finally, it is shown how an effective suppression of jamming and interference is achieved by combining different approaches like application of an adaptive, two frequency antenna array with a post-correlation beamforming, and a robust PVT solution with multi-frequency RAIM.

DISCLAIMER

All information presented and discussed within this paper is part of the public domain. The PRS information used in the paper is freely available e.g. through the GIOVE-A+B Public SIS ICD [1]. No classified documents or information were used. Consequently, the presented receiver will differ in various aspects to real Galileo PRS receivers.

INTRODUCTION

The increasing use of GNSS for military and security related applications is generating a higher demand for robust positioning/navigation solutions. Consequently one of the first Galileo services to become available will be the Public Regulated Service (PRS). Galileo PRS is a special navigation service intended for governmental and governmental authorized users, e.g. police, border control, emergency, armed forces and Search and Rescue (SAR), as well as operators of critical infrastructures like telecommunication- and energy-networks and critical transports. The first PRS signals will be available after the launch of the first Galileo IOV satellites in Autumn 2011. The Public Regulated Service features encrypted signals on two frequency bands with restricted access for specific authorized users as mentioned above. A PRS receiver has to deliver robust, reliable and continuous position information even under challenging reception conditions and also in jammed environments, requiring a

considerable robustness against interference. Furthermore, a protection against signal meaconing and spoofing has to be provided, as well as means to control the use of GNSS signals within a local/regional area of operation. All these issues make a PRS receiver development a very demanding task.

Within the BaSE (Bavarian security receiver) project, a consortium consisting of six Bavarian (Germany) companies and research institutes was formed to investigate core technologies, acquire necessary know-how, and develop a high-end Galileo PRS receiver prototype. The consortium consists of Fraunhofer Institute for Integrated Circuits (IIS), Institute of Communications and Navigation of German Aerospace Center (DLR), IABG, EADS Astrium, NavCert, and Siemens. The project is co-financed and supported by the Bavarian Ministry of Economic Affairs. BaSE has started in February 2010 and will finish with a demonstration of the PRS prototype receiver in January 2012.

Such an efficient cooperation is essential especially for the development of PRS receivers, which is associated with time-consuming processes related not only to security accreditation and certification but also to the subsequent integration of navigation equipment in dedicated platforms with specific environmental and security requirements. Further the use of PRS is (in contrast to GPS PPS) not only limited to military users, but also allowed for other governmental or governmental authorized users. Most of these "new" user communities do not have the same level of experience with security-related equipment as military users; therefore, a dedicated security-architecture has to be chosen to allow a user-friendly handling of PRS-receivers.

The technological objective of BaSE is to develop a flexible and scalable high-performance Galileo PRS prototype receiver. This receiver will operate in the E1 and E6 frequency bands, making use of the Galileo PRS signal components. Special attention is given to robust acquisition and tracking of the BOCc-modulated PRS signals. Effective suppression of jamming and interference is achieved by combining different approaches like application of an adaptive, two frequency antenna array with a post-correlation beamforming. Further objectives are a robust PVT solution (Position-Velocity-Time) with multi-frequency RAIM (Receiver Autonomous Integrity Monitoring) and spoofing detection by estimating direction of arrival.

Other non-technical goals of BaSE are the identification of national users and applications for Galileo PRS, the analysis of their specific requirements, the coordination with national and European PRS interfaces, projects, and developments as well as the elaboration and integration of a capable IT-security concept into the receiver system,

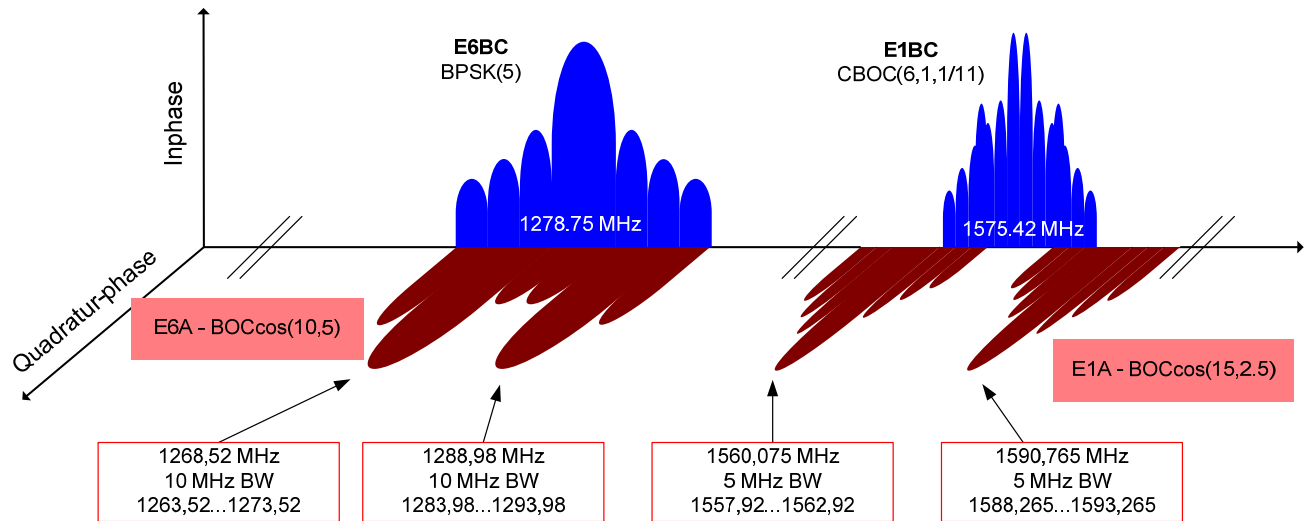


Figure 1: Galileo PRS, CS and OS signals in the E1 and E6 band

and aspects related to future standardization and certification of PRS receivers. Future integration of PRS receivers into the whole Galileo PRS-Management and Security infrastructure are further tasks performed within the BaSE project.

GALILEO PRS SIGNALS

As depicted in Figure 1, the Galileo PRS signals are transmitted over the E1A and E6A frequency bands, using BOCc(15,2,5) and BOCc(10,5) modulation, respectively. BOCc uses a cosine phased subcarrier resulting in higher frequency components than a sine phased subcarrier used in BOCs modulations of e.g. Galileo E1BC Open Service.

As a result, more energy is shifted to the edges of the band what improves the spectral separation with the coexisting OS and CS signals and the theoretical tracking performance. Since the BOCc main-lobes are at the edges of the band, the full transmitted bandwidth should be received [1].

GNSS Signal	Carrier Freq. [MHz]	Modulation	Bandwidth [MHz]
GPS L1 C/A	1575.42	BPSK(1)	2
Galileo E1BC OS	1575.42	CBOC(6,1,1/11)	14
Galileo E1A PRS	1575.42	BOCcos(15,2,5)	40
Galileo E6A PRS	1278.75	BOCcos(10,5)	40

Table 1: GNSS signals tracked by the BaSE receiver

The BaSE receiver is designed to receive and process all signals listed in Table 1.

The Galileo Open Service (OS) signals E1BC are exploited for the acquisition and for the tracking support of Galileo (pseudo-)PRS signals. GPS L1 C/A support is included for on-field demonstrations and for general comparisons with other receivers. The E6BC signals for the planned Galileo Commercial Service (CS) are not used.

The BaSE receiver uses memory codes for the local replica generation. Thus, both GIOVE-B PRS codes [1] can be used, as well as any random sequence provided by an arbitrary waveform signal generator.

BASE RECEIVER HARDWARE

Receiver Hardware Architecture Overview

Figure 2 shows the BaSE receiver block diagram. A self-calibrated, 4-element dual-frequency (E1 and E6) array antenna is used to set the basis for protection against signal meaconing and spoofing with high interference mitigation capabilities. The analog signal conditioning (filtering, amplification, down-conversion) is done in separate quadruple radio frequency (RF) analog front-ends for E1 and E6, respectively. The analog-to-digital conversion (ADC) with digital signal conditioning is carried out in the successive digital front-ends. One digital front-end is used for the four E1 channels and one for the four E6 channels. All necessary clock signals (for the ADCs and the FPGAs) and local oscillator (LO) signals (for the analog mixer stages) are coherently derived and distributed on a dedicated clock and local oscillator generation module. Using an optical multi-gigabit transceiver link (MGT), the digital raw data from the digital front-ends are transferred to the pre-correlation interference mitigation module whose output is finally fed

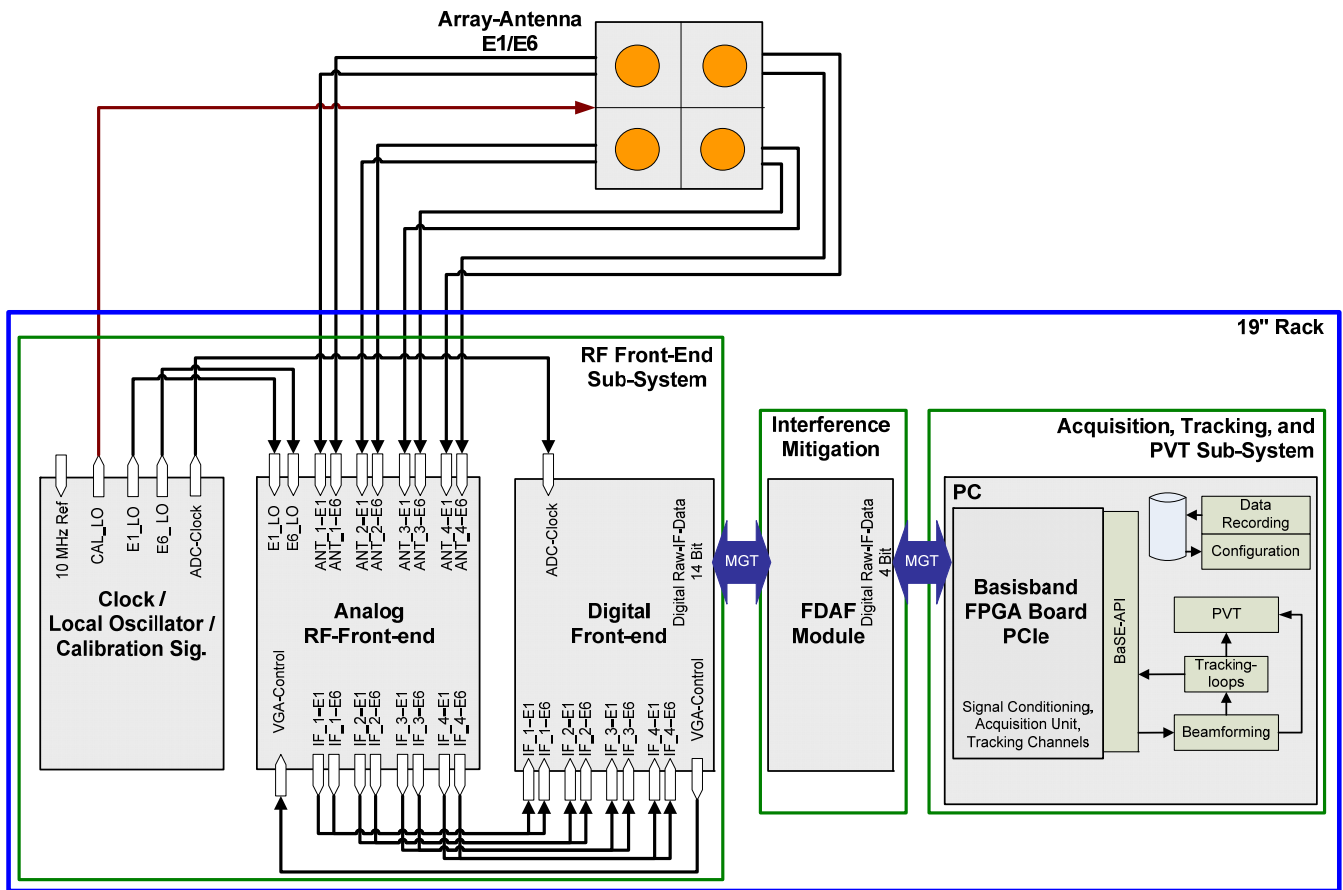


Figure 2: BaSE receiver block diagram

into the baseband receiver hardware, again using an optical MGT. All computationally demanding tasks like, the acquisition and the correlators are implemented on the digital baseband FPGA. The tracking loops are closed in software running on a standard PC over a PCIe link where both the beamforming and the PVT with RAIM and spoofing detection are also implemented.

The hardware setup of the BaSE receiver is depicted in Figure 3, excluding the antenna. The RF front-end sub-system is realized using 6 units of height modules. The interference mitigation module as well as the baseband FPGA are installed within a standard 19" rack PC. An optical cable patch panel gives the possibility to include or exclude the interference mitigation module for different signal combinations. All these components are mounted in a 19" desk chassis using overall 12 units of height.



Figure 3: BaSE receiver setup without antenna

Array Antenna

In order to have both a 4-element dual-frequency antenna and a compact design, the antenna system is based on stacked patch dual-band radiators in a 2-by-2 configuration. The feeding of the dual-output antenna element is designed for high isolation between E1 and E6 signal paths [2]. Simulated realized gain of the antenna element for the desired right hand circular polarization (RHCP) is about 5 dBi for both bands and the suppression of the cross-polarized left hand circular polarization (LHCP) component is at least 15 dB. Individual wide-angle patterns (Figure 4 and 5) and a $\lambda/2$ inter-element distance allows an efficient implementation of the antenna module. Furthermore, to improve the overall axial ratio performance, sequential rotation of elements is foreseen (Figure 6).

The multilayer strip-line approach is intended for embedded calibration networks for each operational band. Therefore, online calibration is possible without dismounting the antenna. Moreover the RF board with amplification and filtering stages is attached underneath the radiators, yielding an integrated solution.

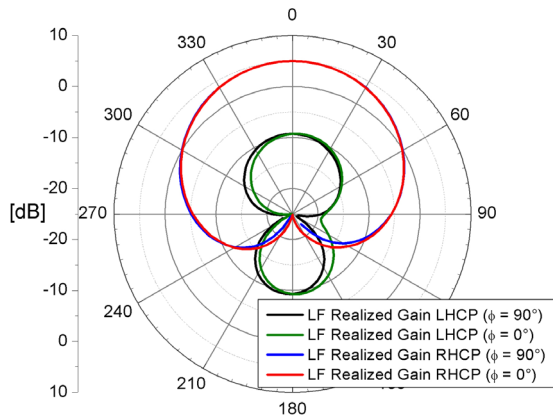


Figure 4: Single antenna element – E6 pattern

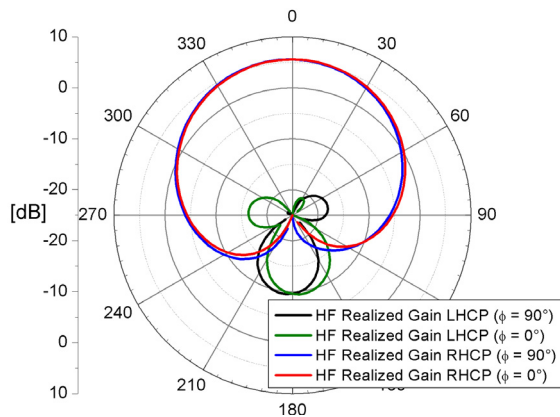


Figure 5: Single antenna element – E1 pattern

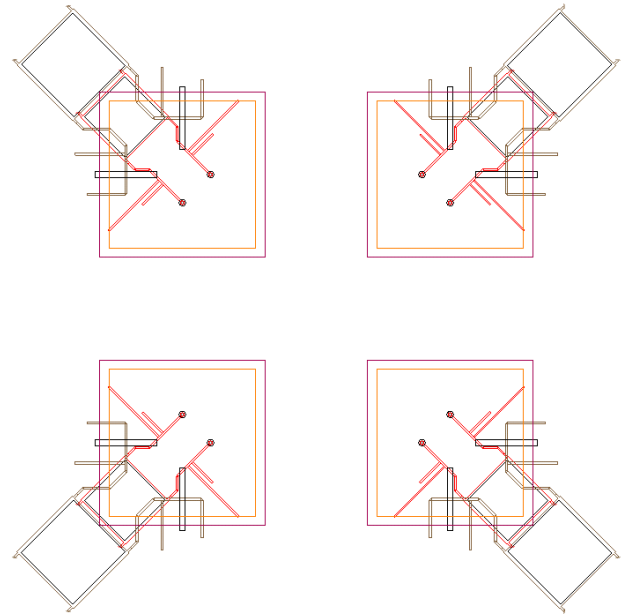


Figure 6: 2x2 Antenna array with sequential rotation

GNSS Front-end Sub-System

The RF front-end sub-system consists of the analog RF front-end boards, a clock/local oscillator generation and distribution unit, and the digital front-end boards.

Analog Front-end

The RF front-ends have to be wideband to process the E1A BOCcos(15,2.5) and E6A BOCcos(10,5) modulated PRS signals and also have to be designed in a very robust way to withstand both out-of-band and in-band interferences.

For both E1 and E6 analog front-ends, a zero-intermediate frequency (IF) architecture was chosen. A zero-IF architecture is very well suited for the BOC modulated Galileo signals, since there is practically no power in the region of the carrier frequency and thus a simple AC-coupling can be used e.g. to remove the typical zero-IF problem of DC-offset due to self-mixing. Thanks to zero-IF there is no need for image rejection, and high quality factor low-pass filters can be used for the band selection providing an excellent out-of-band attenuation.

Figure 7 shows the general architecture of the E1/E6 front-end. RF signal limiters are foreseen after each amplification stage to protect the circuitry from powerful inband jammer with power levels greater than +20 dBm. Either ceramic or surface acoustic wave (SAW) RF filter can be used to enable flexibility in terms of broad bandwidth or high selectivity.

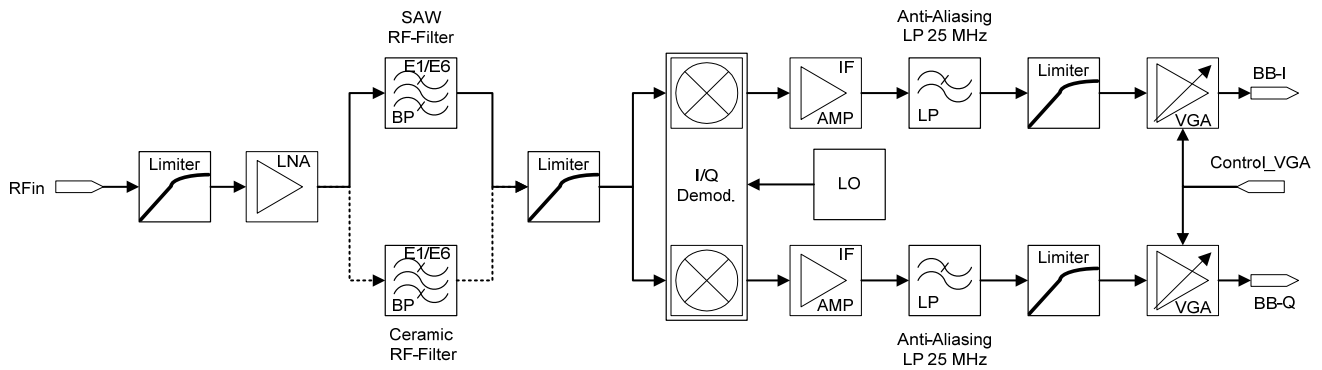


Figure 7: BaSE analog RF front-end architecture

Figure 8 shows the signal down-conversion scheme used. The output of the analog front-end is a complex baseband signal represented with analog inphase and quadrature component signals.

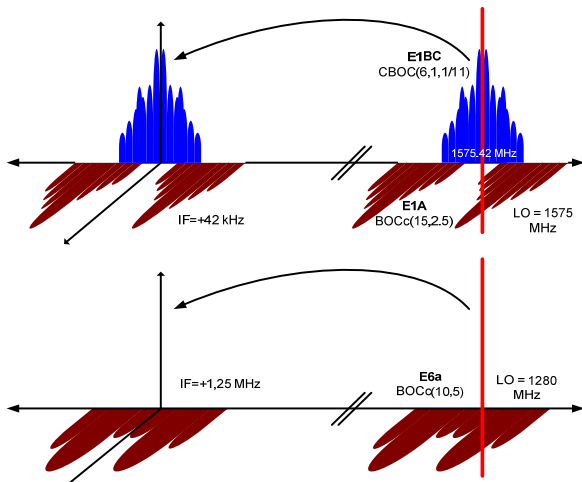


Figure 8: Down-conversion scheme for E1 and E6

A variable gain amplifier (VGA) is used to control the subsequent analog to digital converter (ADC) appropriately. The VGA is controlled via a serial bus by the digital front-end.

Four E1 or E6 analog front-end chains are realized on a single so called E1 or E6 analog RF front-end module, depicted in Figure 9.

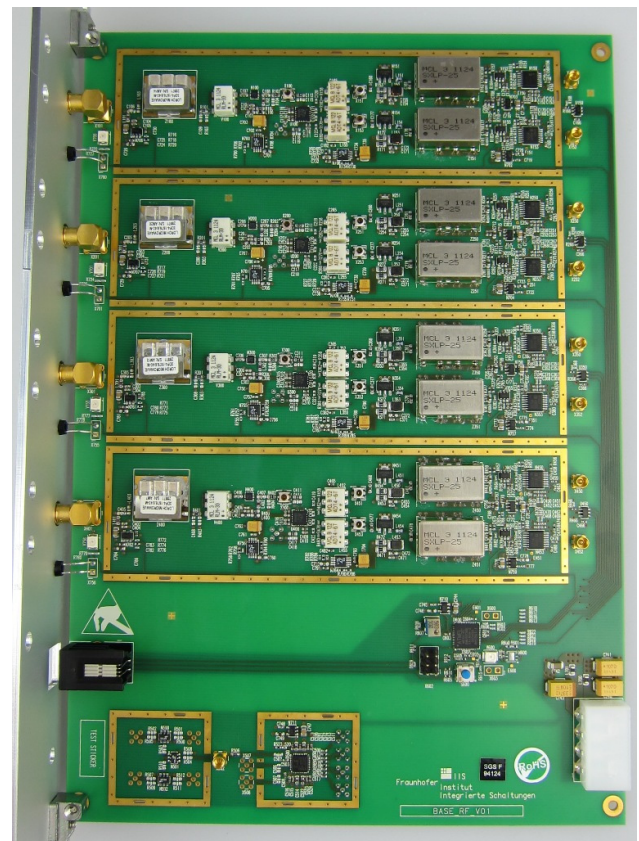


Figure 9: Quadruple analog front-end E1/E6 module

To reduce both the effort of the clock / local oscillator generation and possible interferences coming from different frequency synthesizers, as well as to ensure phase coherence, all frequency synthesizers are derived from a separate clock / LO generation and distribution module and derived from the same reference clock. This approach also allows using an external reference clock if desired.

GNSS Signal	Carrier Freq. [MHz]	LO [MHz]	IF [MHz]
Galileo E1A	1575.42	1575	+0.42
Lower Lobe	1560.075	1575	-14.925
Higher Lobe	1590.765	1575	+15.765
Galileo E6A	1278.75	1280	-1.25
Lower Lobe	1268.52	1280	-11.48
Higher Lobe	1288.98	1280	+8.98

Table 2: Resulting IF frequencies

Table 2 shows the emerging intermediate frequencies when using the proposed local oscillator frequencies. It is generally beneficial to synthesize an LO frequency whose ratio to the reference frequency approaches as closely as possible a rational number (in our case a 10 MHz OCXO) to reduce the phase noise as much as possible.

Digital Front-end

The digital front-end performs the analog to digital conversion, followed by a first signal conditioning, the interference mitigation modules, and the high speed multi gigabit transceiver (MGT) interface for the transmission of the raw IF samples. Its block diagram is shown in Figure 10.

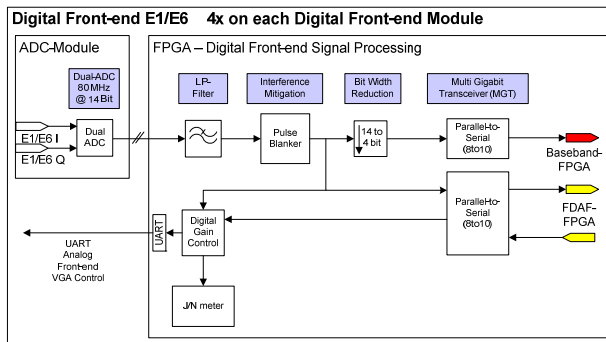


Figure 10: Digital front-end block diagram

High resolution dual-ADCs with 14 bit resolution and 80 MHz sampling rate are used to digitize the complex analog baseband signals and to provide superior mitigation capability against high signal dynamics caused by interferences. Assuming the ADC delivers approx. 12 effective number of bits (ENOB) and using 4 bit for the GNSS-“noise” signals, the remaining 8 bit provide approx. 50 dB of dynamic headroom for e.g. continuous wave interferences quantization without clipping. The chosen sampling rate of 80 MHz is a good trade-off between the effort for the anti-aliasing filter and a still moderate raw data rate.

The digital data stream is processed in an FPGA, which implements different pre-correlation interference mitigation techniques such as pulse blanking and digital filtering. After that, is either a bit width reduction of the digital data before handed over to the baseband FPGA, or

the raw data is directly sent to a dedicated pre-correlation interference mitigation board (FDAF-Module). If the interference mitigation step is successful, the dynamic range can be safely reduced from the initial 14 bit to e.g. 4 bit without any significant implementation loss, since 4 bit are enough for a GNSS noise-like signal with no remaining interferences.

A digital gain control with a jammer-to-noise meter capability finalizes the tasks on the digital front-end FPGA.

Using a similar approach as for the analog front-ends, four E1 or E6 digital front-end chains, consisting of a dual-ADC module, a digital signal processing unit and a MGT for the required 2.24 Gbit/s raw data rate (80 Msamples/s x 14 bits/sample x 2 I/Q components) per reception chain are realized on one so-called E1 or E6 digital front-end module, depicted in Figure 11.

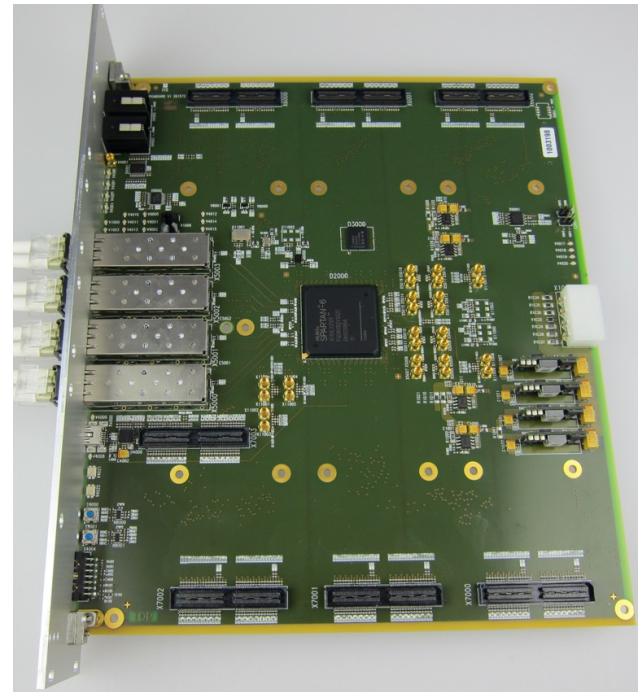


Figure 11: Digital front-end module

Pre-Correlation Interference Mitigation Module

In order to achieve high robustness to radio frequency interference and allow the realization of tracking channels with moderate number of input signal bits, the first stage of the interference mitigation is performed during the signal conditioning directly after the analog to digital conversion (see Figure 10). The mitigation is based on the frequency domain adaptive filtering (FDAF) approach [3]. The conversion of the digitalized signals into the frequency domain is performed using an FFT with a length of 1024 samples. The frequency bins having significantly higher levels than the average noise floor are assumed to contain the interference energy and therefore

are nulled out. Before further processing, the signal is converted back to the time domain with the help of an inverse FFT. The techniques can be effectively implemented for block processing in real time and allows mitigating radio interference with compact frequency content such as narrowband or pulsed signals.

Further radio interference mitigation is performed after the PRN code correlation with the help of adaptive beamforming. The BaSE PRS receiver uses the pre- and post-correlation techniques in a flexible way depending on the actual interference situation and the application in hand.

Baseband Sub-System

The baseband module consists of an FPGA, where the hardware signal conditioning, the hardware FFT acquisition block and the tracking correlators are implemented, and a PC where the baseband signal processing algorithms are executed. Its block diagram is shown in Figure 12. The interface to the front-end sub-system and/or the interference mitigation module is implemented via eight optical MGT, providing a maximum raw data throughput of 17.92 Gbit/s (four E1 and four E6 raw data streams with 2.24 Gbit/s each). The interface to a standard PC is realized over a high-speed PCIe connection.

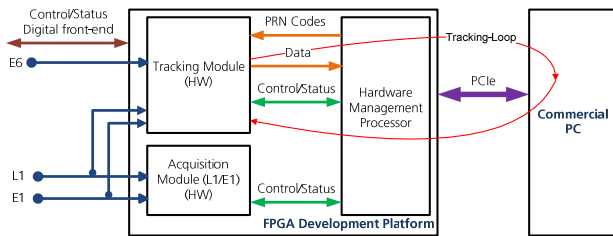


Figure 12: Hardware assisted software tracking

Using an application programming interface (API) the baseband FPGA can be controlled and the tracking loops closed in software. This approach uses the advantages of the fast parallel FPGA processing while still providing the flexibility of a software receiver. Table 3 provides some exemplary BaSE-API functions with their descriptions that can be used in the tracking control software.

start_baseband() stop_baseband()	Start/stop the baseband hardware
set_integr_time()	Set the integration time in ms for one beamforming channel
acquisition()	Requesting the acquisition with controlling parameters and returning the acquisition result
register_tracking_cb()	Registers a callback function to be called when new correlation results are available
apply_nco_parameters()	Apply NCO parameters using the provided control values

register_pr_measurement_cb()	Registers a callback function to be called when new pseudorange measurements are available
to_bf_ch()	Beamforming channel to hardware channel conversion

Table 3: Exemplary BaSE-API functions

Four hardware tracking channels form a so-called beamforming channel, as depicted in Figure 13. The mapping of the physical tracking channels to one logical beamforming channel is controlled by the software using the BaSE-API. For each satellite and frequency such a quadruple beamforming channel is necessary. With a maximum of 11 Galileo space vehicles (SV) in view, tracked on 2 frequencies (E1A and E6A) with 4 antenna elements for each frequency band, 88 hardware tracking channels should be implemented in the digital baseband FPGA.

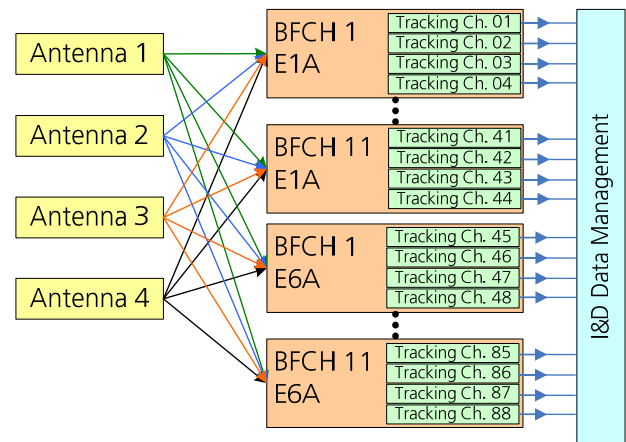


Figure 13: Combination of 4 tracking channels to a beamforming channel (BFCH)

BASEBAND SIGNAL PROCESSING

Acquisition

A hardware acquisition unit with an FFT based time correlation approach is used. This guarantees a quick two-dimensional search for GPS L1 C/A and Galileo E1B/C signals regarding code offset and Doppler frequency offset. The acquisition unit is controlled by the hardware management processor, which configures the module with the satellite PRN, Doppler bin, coherent and non-coherent integration time. Outputs of this unit are peak position (code offset) and peak magnitude after a successful detection.

Double Estimator Tracking

Different tracking algorithms have been considered to address the challenges inherent to the ambiguous PRS signals' correlation functions. In particular, Multiple Gate Delay Discriminators, BPSK-like techniques, conventional E-L tracking in combination with a bump-jump algorithm, and the Double Estimator [4] have been

compared with respect to their hardware complexity, computational load, tracking accuracy, multipath performance, and robustness against dynamics. Finally, a slightly modified version of the Double Estimator was selected to be implemented in the receiver prototype, as this technique almost achieves the same performance as a conventional E-L tracking, without the practical problems frequently encountered on bump-jumping, and with hardware and processing capabilities requirements significantly less stringent than other techniques.

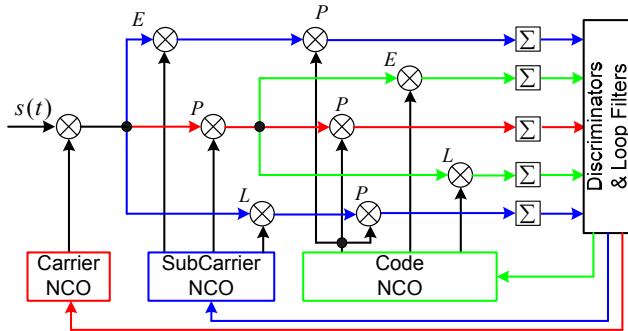


Figure 14: Double Estimator Architecture

A block diagram of the Double Estimator architecture is shown in Figure 14, which consists of three loops: the phase lock loop (PLL) for carrier tracking, the delay lock loop (DLL) for code tracking, and an additional loop not present in a conventional BPSK tracking architecture, i.e. the subcarrier lock loop (SLL) for subcarrier tracking.

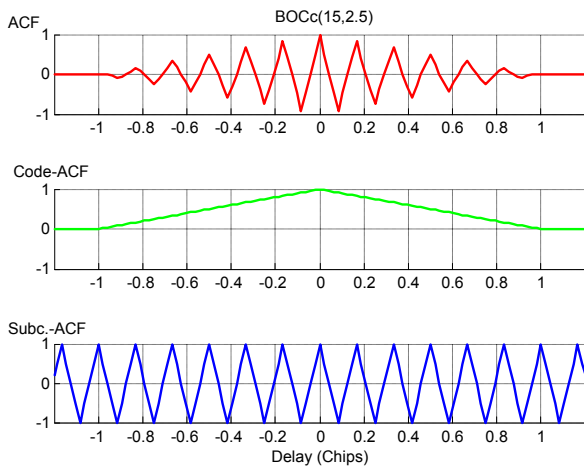


Figure 15: ACFs of Code, Subcarrier, and complete Signal shown for the E1A

The PLL provides the carrier wipe-off required for DLL and SLL, and is used to obtain carrier phase measurements. The correlation with a subcarrier prompt replica provides a subcarrier wipe-off, which allows

correlating the resulting signal in the DLL with early and late code replicas for code tracking. The subcarrier tracking is achieved after carrier wipe-off by correlating with early and late subcarrier replicas, and a code wipe-off using the prompt code replica from the DLL. As in a conventional BPSK receiver where the PLL and DLL can be seen as almost independent – a typical code tracking error still allows to achieve the code wipe-off required for carrier tracking – the Double Estimator PLL, DLL, and SLL are basically independent, too, in the same sense that limited tracking errors in one of the three loops do not propagate directly in the two other loops. So, besides the carrier phase, the Double Estimator provides two independent range measurements, a highly accurate but ambiguous range from the SLL, and an unambiguous but less accurate range from the DLL. Usually, a rounding operation is used to combine these two ranges to a final, highly accurate and unambiguous pseudorange. So contrary to a conventional early-late tracking of PRS signals, no explicit bump-jumping algorithm is required. Furthermore, the Double Estimator architecture can be easily modified to allow for BPSK tracking, too, simply by not correlating with a subcarrier replica. This is very beneficial especially for the BaSE PRS receiver, which needs to support GPS L1 C/A, too.

Beamforming and Direction Estimation

The beamforming and direction estimation algorithms are used to optimize the signal-to-noise-plus-interference ratio (SNIR) for the navigation signals making the PRS receiver more robust, as well as to distinguish the legacy signals from spoofing with the help of the arrival directions. The array processing is performed in the software part of the receiver after the PRN-code correlation (see Figure 17), i.e. after de-spreading operation. With this approach the algorithms are operating at relatively low signal rates, which enable the realization of a wide range of algorithms from simple to very complex ones in a real-time receiver platform. A block diagram of a single receiver tracking channel with the post-correlation array processing is shown in Figure 16. Two kinds of array processing are going to be used in the BaSE platform: (i) digital beamforming with the adaptive null-steering based either on minimum variance or minimum mean squared error optimization criteria (see [5] and [6] for more details) and (ii) the estimation of signal directions of arrival (DOA) with the help of unitary ESPRIT algorithm [7]. The direction estimation is going to be used in a modified RAIM approach that accounts for assisting directional information about the received navigation signals.

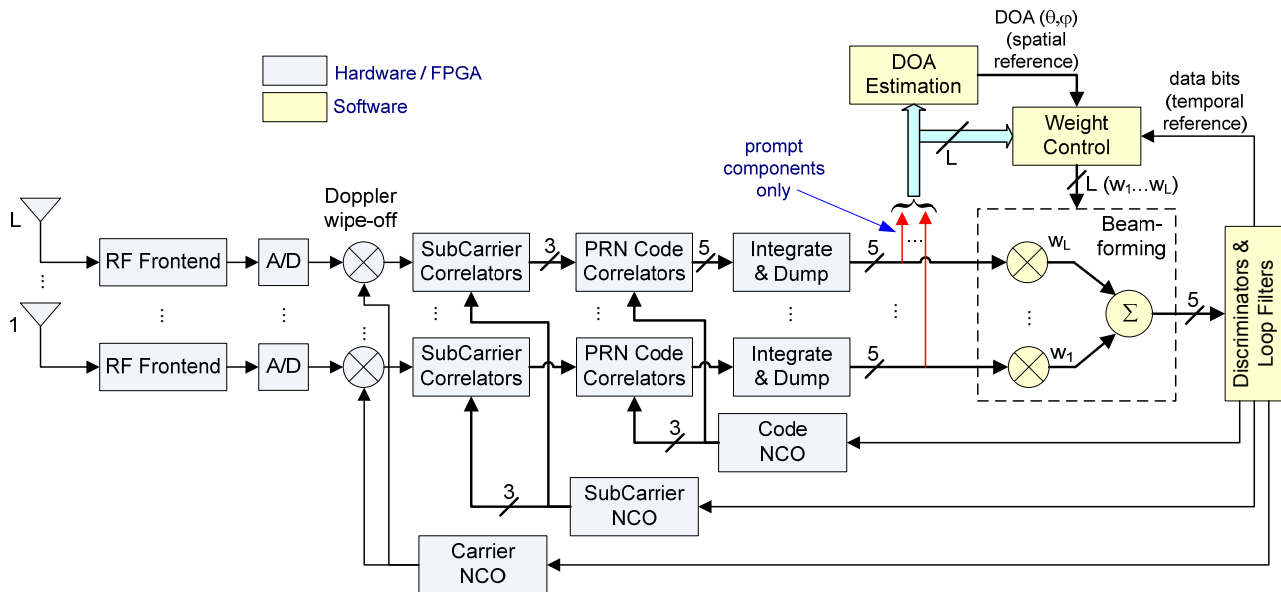


Figure 16: Block diagram of digital beamforming and direction-of-arrival estimation after PRN code correlation for a single beamforming channel of the BaSE receiver

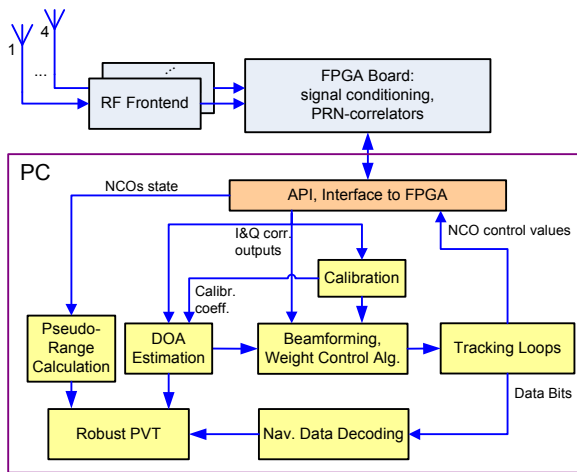


Figure 17: Architecture of receiver software

PVT and RAIM

The positioning solution of the PRS receiver utilizes both code- and carrier-range measurements. The availability of the double-frequency E1/E6 measurements allows the use of an ionosphere-free combination that is robust against a non-modeled ionosphere range error. The integrity check of the obtained positioning solutions is based on the dual-frequency Receiver Autonomous Integrity Monitoring (RAIM) as well as on the additional information about the directions of arrival of the involved navigation signals (see Figure 17).

CONCLUSION

The BaSE project will enhance the competitiveness of the German industry in the field of high-performance satellite navigation and security systems. It will allow early testing of the integration of PRS-receivers into the Galileo PRS-Management/Security-architecture and will provide the basis for future certification of PRS receivers. The close link between research institutes, industrial partners and certification organizations will allow a fast and effective migration from prototypes into products.

ACKNOWLEDGMENTS

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